CLAIM AMENDMENTS:

1. (Currently amended) A semiconductor device comprising:

a semiconductor substrate;

an insulating layer disposed on said semiconductor substrate;

an SOI film disposed on said insulating layer;

a gate insulator disposed on said SOI film; and

a gate electrode disposed on said gate insulator;

wherein a source, a drain, and a channel are formed in said SOI film so that said gate insulator is located at least between said channel and said gate electrode, thereby forming a MOSFET including said source, said drain, said channel, said gate electrode, and said gate insulator; and

wherein said gate electrode is made of P-type polysilicon and conductivity types of said source, said drain, and said channel are all N-type, an N-type impurity concentration in said channel is ~~within a range approximately from 1×10^{17} cm^{-3} to 1×10^{18} cm^{-3}~~ approximately 3×10^{17} cm^{-3}, and a channel length of said channel is ~~within a range approximately from 0.1 μm to 0.25 μm~~ approximately 0.15 μm.

2. (Cancelled)

3. (Cancelled)

4. (Original) The semiconductor device according to claim 1, wherein a thickness of said gate insulator is within a range approximately from 1 nm to 4 nm, and a thickness of said SOI film is within a range approximately from 10 nm to 40 nm.

5. (Original) The semiconductor device according to claim 4, wherein said thickness of said gate insulator is approximately 2 nm, and said thickness of said SOI film is approximately 20 nm.

6. (Original) The semiconductor device according to claim 1, wherein said source and said drain are doped with N-type impurities so that an N-type impurity

concentration in said source and said drain is not less than approximately 1×10^{21} cm^{-3}.

7. (Cancelled)

8. (Cancelled)

9. (Currently amended) A metal-oxide-semiconductor field-effect transistor comprising:

a semiconductor substrate having a substrate, an insulating layer which is disposed on the substrate and a silicon layer which is disposed on the insulating layer;

a gate insulator disposed on the silicon layer of the semiconductor substrate;

a gate electrode, which is made of P-type polysilicon, disposed on the semiconductor substrate so that the gate insulator is disposed between the gate electrode and the semiconductor substrate;

a channel region formed in the silicon layer, which is located under the gate electrode; and

a source and a drain formed in the silicon layer and being adjacent to the channel region;

wherein said gate electrode is made of P-type polysilicon and conductivity types of said source, said drain, and said channel are all N-type, an N-type impurity concentration in said channel is ~~within a range approximately from 1×10^{17} cm^{-3} to 1×10^{18} cm^{-3}~~ approximately 3×10^{17} cm^{-3}, and a channel length of said channel is ~~within a range approximately from 0.1 μm to 0.25 μm~~ approximately 0.15 μm.

10. (Cancelled)

11. (Cancelled)

12. (Original) The metal-oxide-semiconductor field-effect transistor according to claim 9, wherein a thickness of the gate insulator is within a range approximately from 1 nm to 4 nm, and a thickness of the silicon layer is within a range approximately from 10 nm to 40 nm.

13. (Original) The metal-oxide-semiconductor field-effect transistor according to claim 12, wherein the thickness of the gate insulator is approximately 2 nm, and the thickness of the silicon layer is approximately 20 nm.

14. (Original) The metal-oxide-semiconductor field-effect transistor according to claim 9, wherein the source and the drain are doped with N-type impurities so that an N-type impurity concentration in the source and the drain is not less than approximately 1×10^{21} cm^{-3}.

15. (Cancelled)

16. (Cancelled)